**R09**

**Code No: D3805, D0602, D7005, D5505, D7709, D6809, D5709**

**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD**

**M.TECH II - SEMESTER EXAMINATIONS, APRIL/MAY 2012**

**LOW POWER VLSI DESIGN**

**(COMMON TO DIGITAL ELECTRONICS & COMMUNICATION SYSTEMS, DIGITAL SYSTEMS & COMPUTER ELECTRONICS, ELECTRONICS & COMMUNICATION ENGINEERING, EMBEDDED SYSTEMS, EMBEDDED SYSTEMS & VLSI DESIGN, VLSI & EMBEDDED SYSTEMS, VLSI SYSTEM DESIGN)**

**Time: 3hours** **Max. Marks: 60**

**Answer any five questions**

**All questions carry equal marks**

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1.a) What are the Low-Voltage, Low-Power design considerations? Explain.

b) Explain about SOI Technology with necessary sketches.

2.a) Draw the structure for optimized twin-well BICMOS with self aligned $p^-$ and $n^+$ buried layers for improved packing density and explain the same.

b) What are the BICMOS manufacturing and integration considerations? Explain.

3.a) Explain about LOCOS process and Advanced Isolation Technologies.

b) Draw the structure for polysilicon, emitter high-performance BICMOS and explain the same.

4.a) What is the need for Copper in Integrated Circuits? What are the steps in Copper metallization? Explain.

b) What are the future trends and directions in CMOS/BICMOS processes? Explain.

5.a) Explain about different BSIM models for MOSFETs.

b) Explain about EKV MOSFET Model and HICUM Bipolar Transistor Model.

6.a) Explain about basic driver circuits for BICMOS logic gates and explain their operation.

b) Draw the circuit for High-Performance Complimentary Coupled BICMOS circuit for 3 input NAND and explain its working.

7. Draw the circuit for R-type, N-type and R+N type BICMOS Inverters and explain about their working. Compare them in all respects.

8. Write Notes on any TWO

a) Quality measures for Flip-Flops

b) Design aspects of Low power latches

c) FSCMBL two input NAND gates.

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